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Over the last 30 years, IC complexity has grown from small scale integration to very large scale integration, while hybrid interconnect technology has not. As a result, a considerable gap in performance between bare die and conventionally packaged electronic devices has emerged. In order to address and overcome this electronic interconnect bottleneck, POC investigated the architectural design and component issues concerning high density electrooptic packaging technology. Specifically, the following major areas were studied, with a special emphasis on electrooptic modulator fabrication, material processing, and long term thermal stability and survivability of the $\chi^{(2)}$ material based NLO polymer modulators: (i) investigation of high density hybrid packaging; (ii) study of different modulator designs, fabrication methods, and simulated modulator topology; (iii) study of NLO polymers with high EO coefficients; (iv) fiber optic connectorization; and (v) software development.

Based on our studies, we have concluded that an enormous application potential exists for both the EO modulator as an individual component and the high density chip packaging technology for the communication industry. Further development and testing are needed to complete the efforts initiated in Phase I.

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1.0 INTRODUCTION

The state-of-the art in electronics, ICs, and electrical interconnects has reached its limit in both clock speed and in the amount of data that can be processed in a single clock cycle. Clock speed is limited by clock skew, clock delay, and the many different path (track) lengths that an electrical signal must take in a PC board. The amount of processable data is limited by the number of pins on a high density IC package. For example, in state-of-the-art electronic printed circuit boards (PCBs), or even multichip module (MCM) packaging, the speed-distance product and pin count are 5 GHz·cm and 500 pins per chip, respectively. Unfortunately, this figure of merit is much lower than what is immediately required to complete highly complex calculations for both military and commercial applications (such as the modeling of turbulent flow over textured surfaces on missiles, bullets, fighter jets, rockets, etc.), and for the fast and accurate prediction of weather patterns. Furthermore, current and projected electronic solutions offer only marginal or incremental improvements in speed and packaging, and thus will not fulfill the speed, distance, pin count, and density requirements of current and future imaging and data processing systems. Such systems include image processors used in rapid target recognition and missile interception; medical image processing; high definition TV (HDTV) image compression; and ultra high-speed communication network switching related to Asynchronous Transfer Mode (ATM) schemes.

In order to address and overcome this electronic interconnect bottleneck, hybrid optoelectronic interconnects must be incorporated into existing electronic ICs through innovations in packaging process technology. Hybrid optoelectronic interconnects can reduce propagation delays and significantly help in eliminating the problems of RC time constants, inductive noise between lines, and line capacitance. An important advantage of hybrid interconnects is their ability to multiplex many signals onto a single optical medium (like fiber), creating a virtual data channel equivalent to a large number (> 100) of electronic pins. This dramatically improves processing speed, clock distribution, and packaging density, and as a result, highly efficient use of PCB real estate is made possible. Despite these important advantages, little commercial progress has been made in this area, especially at the chip level. This is because an electrooptic (EO) modulator (a key component in hybrid optoelectronic interconnects) is not commercially available at the VLSI scale of integration. In addition, most EO modulators are not compatible with standard VLSI fabrication processes, making the chip level integration of optics and electronics prohibitively expensive.

Recent developments in polymeric materials have made it possible to integrate silicon substrates with electronic dies and waveguides. Because Physical Optics Corporation (POC) has been involved in the research, development, and manufacturing of waveguide modulators, fiber optic communication links, optical interconnects, multichip module packaging, and EO material processing, we are able to offer optimum and cost effective solutions to alleviate the current bottlenecks in electronic interconnects. We do this by integrating EO modulators at the chip level.

Despite the close relationship between hybrid interconnections and integrated circuit (IC) development, IC complexity over the last 30 years has advanced from small-scale integration to very large-scale integration (with more than 10^5 components per circuit), while hybrid interconnection technologies have not . Consequently, a considerable gap in performance has emerged between bare die and conventionally packaged electronic devices. Figure 1-1 shows the clock frequency difference between bare die and conventionally packaged chips. This performance gap will only grow wider unless there is considerable improvement in interconnection technology.

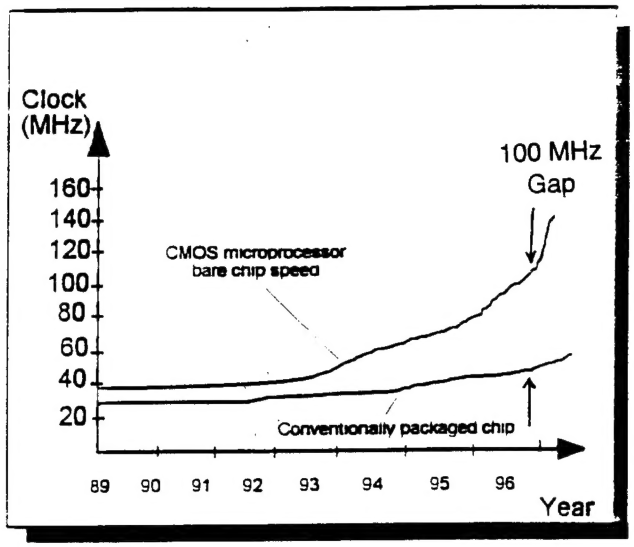
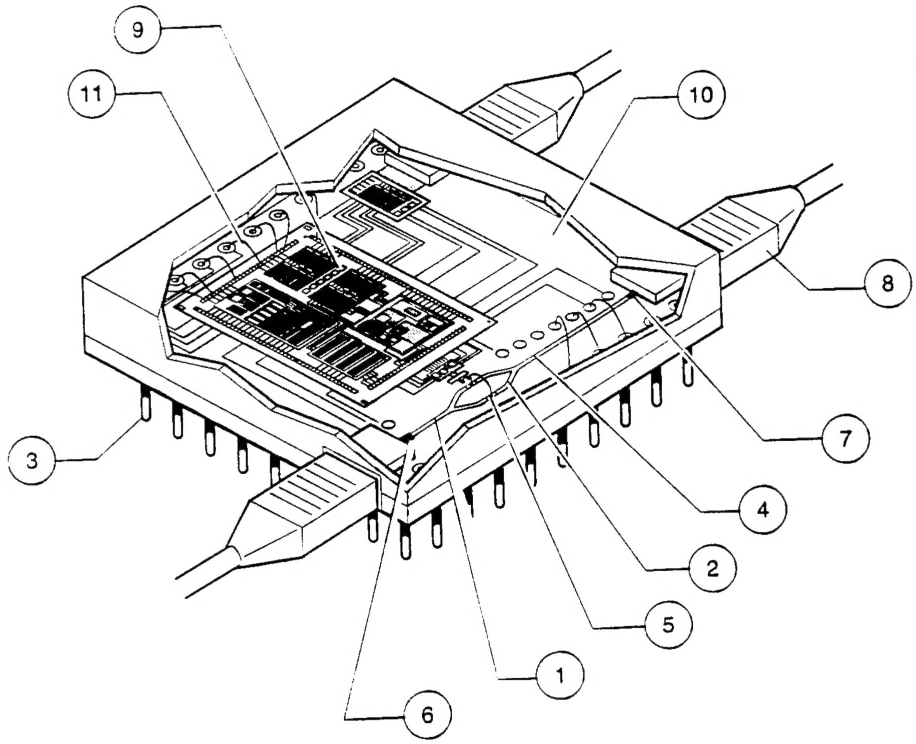


Figure 1-1
Bare die vs. packaged chip clock speed. This clock speed difference will only grow wider unless there is considerable improvement in interconnect technology, such as optical interconnect.

Moreover, there is an immediate need to match the bare die vs. packaged chip clock speed. In order to accomplish this, POC investigated a new *Ultra-Virtual Density Opto-electronic Packaging (UV-DOP) technology*. EO polymers, waveguide structures, system design, and real-estate issues pertaining to compact packaging were investigated.

The uniqueness of virtual density packaging lies in its ability to carry information corresponding to a large number of electrical pins over a single optical multichannel data link applied to chip-to-chip communications on a PC board. The system architecture that was studied during Phase I is illustrated in Figure 1-2.

This system solution investigated in Phase I provided substantial reductions in IC fabrication complexity by dramatically reducing the number of IC pins (by one order of magnitude or more; the cost of electronic ICs is directly proportional to the number of pins). Some state-of-the-art ICs can have as many as 500-600 pins; with POC's UV-DOP approach the pin count can be reduced to 50-60. In this case, an entire data bus of 128 pins (e.g., as in graphic accelerators) can be multiplexed using a single optical line. Additionally, this solution carries substantial savings in PCB real estate because only one optical data path is used rather than the large number of electronic lines of a conventional package. It must be stressed that POC's UV-DOP solution is based on a low cost and mature external EO modulator technology, previously proven feasible for this application in Phase I of this project. The combination of an EO modulator at the chip level with fiber optic data multiplexing at the board level will bring a new level of performance in integrated electronic systems. In general, fiber optic communications have been used for long-haul transmission lines, but in recent years, fiber optic applications have expanded to short-haul transmission, as in local area networks (LANs) (such as FDDI, ATM, and Ethernet).



Legends

1. Mach-Zehnder modulator (input arm)
2. Mach-Zehnder modulator arm
3. Standard metallic I/O pins
4. Mach-Zehnder output arm
5. Modulator electrodes
6. Input fiber tip
7. Output fiber tip
8. Fiber connector
9. Electric IC die
10. SiO_2 substrate
11. Wire bonding of the IC to the substrate

Figure 1-2
Illustration of the System Architecture That was Studied During Phase I of this Program.

1.1 Benefits of POC's Technology

1. **Density.** Electronic packaging and interconnections are planar or quasi-planar, and cannot overlap or cross without proper insulation. In contrast, UV-DOP based optical interconnections can provide a much greater density of interference-free interconnections-up to 1000 interconnects/cm.
2. **Delay**. Photons travel at the speed of light (0.3 mm/ps in free-space). The propagation time delay is thus 3.3 ps/mm. By comparison, propagation delays of electrical signals in striplines fabricated on ceramics and polyimides are approximately 10.2 and 6.8 ps/mm, respectively.
3. **Bandwidth.** The density of UV-DOP-based optical interconnections is not affected by the bandwidth of the data carried by each connection. This is not the case in electronics, where the density of interconnections must be sharply reduced at high modulation frequencies to eliminate capacitive and inductive coupling effects between proximate interconnections. Optical interconnections therefore have greater density-to-bandwidth products than those of electronic interconnections.

4. **Power.** Electrical transmission lines used in current packaging must be terminated with matched impedance to avoid signal reflections. This usually requires a larger expenditure of power. With the UV-DOP-based interconnections, the power requirements are only limited by the sensitivity of the photodetectors and the efficiencies of the electrical-to-optical and optical-to-electrical conversions.

2.0 PHASE I RESULTS

Phase I efforts focused on the following major areas of this program:

- Investigation of the ultra-virtual density optical packaging (UV-DOP) technology.
- Study of different modulator designs, fabrication methods in conjunction with the UV-DOP technology, and a simulated modulator topology.
- Review of an EO modulator that offers high EO coefficients at high temperature stability.
- Software development for the design of the multilayer architecture for the waveguide modulator (see Appendix A for software listing).
- Experimental study of EO modulator fabrication and testing procedures.
- Study of fiber optic connectorization and fiber waveguide coupling methods.

The relevant results of Phase I as they relate to Phase II are given in the following sections.

2.1 Technology Evaluation

Electronic technologies are increasing in capability at an ever faster rate. However, the corresponding packaging technology lags far behind. The processing speed of integrated circuits (ICs) is doubling every five years due to increases in the clock speed and the width of the data processed in a single clock cycle. The major clock speed limitations (such as clock skew, clock delay, and uneven path lengths) have become critical issues for clock speeds in excess of 100 MHz (internal IC clock speed). The situation becomes even more critical if the data is transferred from one IC to another over several inch distances. The speed distance product of the electrical interconnections reaches its technological limit at 4.5 GHz cm. One solution is to increase the processing power of electronic ICs by processing wider data words in a single clock cycle. Currently, some cutting-edge graphic accelerators can process 192 bit words in a single step. However, this solution is highly impractical, given the high real estate needed to provide wide-bus interconnectivity and multiplexing; e.g., a 192 lines wide bus with 0.008" track separation will need more than 1.50" to accommodate the bus on a printed circuit board (PCB). Furthermore, the pin count for a single IC has reached a limit of 500 - 600 pins. The introduction of the virtual optical pin concept will solve most real estate problems of an IC, as well as increase its data/address bus multiplexing capabilities.

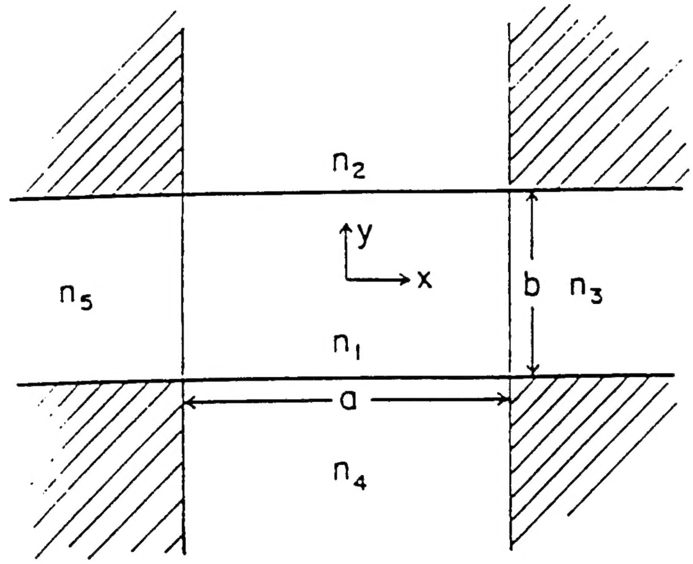
2.2 Software to EO Modulator Multilayer

The design of the EO modulator requires the involvement of computer design tools to define the structure of the modulator, simulate the integration of the EO modulator with the waveguide, and optimize the modulator waveguide multilayer structure. In Phase I of this program, POC developed a design integration software (DIS) that can be used in the design, analysis, and optimization of the multilayer structure, including the active EO material layers. In particular, the software can be used for channel waveguide EO

modulator structure design, multilayer active/passive structure design, and optimization of the waveguide EO modulator layer structure and thickness.

The software is based on dielectric waveguide theory for channel waveguide structures by using Marcatili's method. The solution derived here is very useful in designing rectangular three-dimensional waveguides.

The basic rectangular channel waveguide structure consists of a waveguide region of index n_1 surrounded on all sides by confining media of lesser index n_2, n_3, n_4, and n_5, respectively (Figure 2-1). The indices of the confining media do not have to be the same. However, the same confining media give rise to the symmetric modes in the waveguide.



$n_1 > n_2, n_3, n_4, n_5$

Figure 2-1
Illustration of Basic Rectangular Channel Waveguide Structure

The exact solution of the wave equation for this general case is extremely complicated and too difficult to obtain. However, by using Marcatili's method, an approximate solution can be derived. We are assuming that the modes are well guided so the field decays exponentially in regions 2,3,4, and 5, with most of the power being confined to region 1. The magnitudes of the fields in the shaded corner regions of Figure 2-1 are small enough to be neglected. Hence, Maxwell's equations can be solved by assuming relatively simple sinusoidal and exponential field distribution, and by matching boundary conditions only along the four sides of region 1.

We know the guided modes can be grouped into two families, E^x_{pq} and E^y_{pq}, where the mode numbers p and q correspond to the number of peaks in the field distribution in the x and y directions, respectively. The transverse field components of the E^x_{pq} modes are E_x and H_y, while those of the E^y_{pq} modes are E_y and H_x. The fundamental mode E^y_{11} is sketched in Figure 2-2. The shape of the mode is characterized by extinction coefficients η_2, ξ_3, η_4, and ξ_5 in the regions where it is exponential, and by propagation constants k_x

and k_y in region 1. The η_2, ξ_3, η_4, and ξ_5 measure the 'penetration depths' of the field components in the media 2, 3, 4, and 5, respectively.

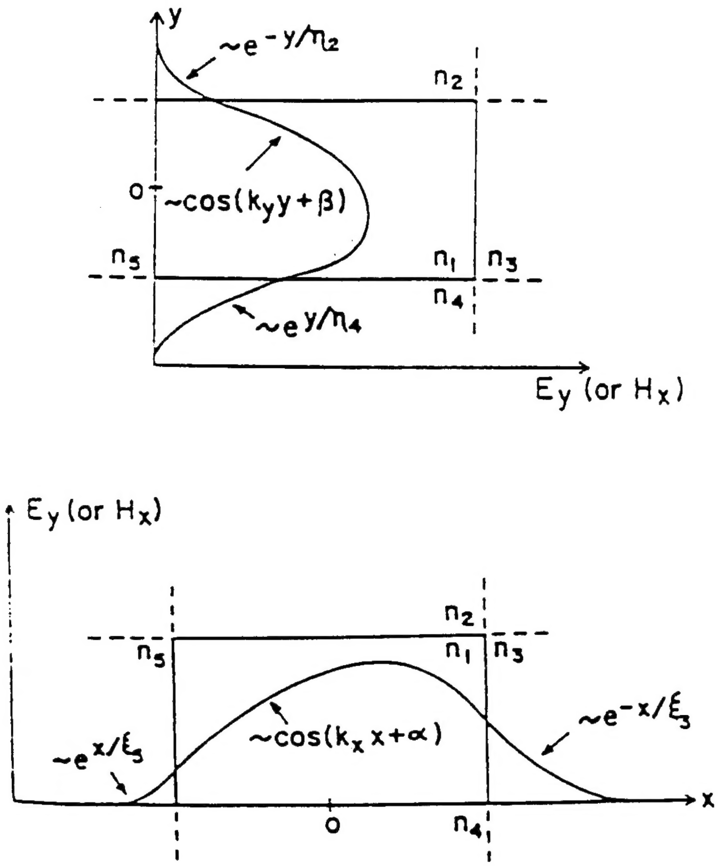


Figure 2-2
Illustration of Fundamental Mode of Guided Wave Characterized of Extinction Coefficient η_2, ξ_3, and ξ_5, which were Used to Measure the Penetration Depth

Quantitative expressions for k_x, k_y, η and ζ can be determined for the E^y_{xy} modes as follows. The field components in the five regions shown in Figure 2-1 designated by v = 1, 2, 3, 4, 5 have the form:

$$
\begin{aligned}
H_{xy} &= \exp(\text{-}ik_z z + i\omega t)\, M_1 \cos\left(k_y + \alpha\right) \exp\left(-ik_{x3}x\right) \quad \text{for } v = 1 \\
H_{xv} &= \exp(\text{-}ik_z z + i\omega t)\, M_2 \cos\left(k_y + \alpha\right) \exp\left(-ik_{x3}x\right) \quad \text{for } v = 2 \\
H_{xv} &= \exp(\text{-}ik_z z + i\omega t)\, M_3 \cos\left(k_y + \beta\right) \exp\left(-ik_{x3}x\right) \quad \text{for } v = 3 \\
H_{xv} &= \exp(\text{-}ik_z z + i\omega t)\, M_4 \cos\left(k_y + \alpha\right) \exp\left(-ik_{x3}x\right) \quad \text{for } v = 4 \\
H_{xv} &= \exp(\text{-}ik_z z + i\omega t)\, M_5 \cos\left(k_y + \beta\right) \exp\left(-ik_{x3}x\right) \quad \text{for } v = 5
\end{aligned}
\qquad (2\text{-}1)
$$

$$H_{yv} = 0 \tag{2-2}$$

$$H_{zv} = \frac{i}{k_z} \frac{\partial^2 H_{xv}}{\partial x \, \partial y} \tag{2-3}$$

$$E_{xv} = -\frac{1}{\omega \varepsilon_o n^2{}_v k_z} \frac{\partial^2 H_{xv}}{\partial x \, \partial y} \tag{2-4}$$

$$E_{yv} = -\frac{k^2 n^2{}_v - k^2{}_{yv}}{\omega \varepsilon_o n^2{}_v} H_{xv} \tag{2-5}$$

$$E_{zv} = \frac{i}{\omega \varepsilon_o n^2{}_v} \frac{\partial H_{xv}}{\partial y} \tag{2-6}$$

where M_v is an amplitude constant, ω is the angular frequency and ε_0 is the permitivity of free space. The phase constants α and β locate the field maxima and minima in region 1, and k_{yv} (v=1,2,3,4,5) are the transverse propagation constants along the x and y directions in the various media. Matching the boundary conditions requires the assumption that

$$k_{x1} = k_{x2} = k_{x4} = k_{x,}, \tag{2-7}$$

and

$$k_{y1} = k_{y2} = k_{y4} = k_y, \tag{2-8}$$

also,

$$k_z = \left(k_1{}^2 - k_x{}^2 - k_y{}^2\right)^{1/2}, \tag{2-9}$$

where

$$k_1 = kn_1 = 2\pi n_1 / \lambda_0, \tag{2-10}$$

is the propagation constant of a plane wave with free-space wavelength $\lambda_0$in a medium of refractive index n_1.

Matching field components at the boundaries of region 1 yields the transcendental equations

$$k_x a = p\pi - \tan^{-1} k_x \zeta_3 - \tan^{-1} k_x \zeta_5, \tag{2-11}$$

and

$$k_y b = p\pi - \tan^{-1} \frac{n_2{}^2}{n_1{}^2} k_y \eta_2 - \tan^{-1} \frac{n_4{}^2}{n_1{}^2} k_y \eta_4 \tag{2-12}$$

where the $\tan^{-1}$ functions are to be taken in the first quadrant, and where

$$\zeta 3 = \frac{1}{k_{x3}} = \frac{1}{\left[\left(\frac{\pi}{A_3}\right)^2 - k_x^{\,2}\right]^{1/2}} \tag{2-13}$$

$$\zeta 5 = \frac{1}{k_{x5}} = \frac{1}{\left[\left(\frac{\pi}{A_5}\right)^2 - k_x^{\,2}\right]^{1/2}} \tag{2-14}$$

$$\eta 2 = \frac{1}{k_{y2}} = \frac{1}{\left[\left(\frac{\pi}{A_2}\right)^2 - k_y^{\,2}\right]^{1/2}} \tag{2-15}$$

$$\eta 4 = \frac{1}{k_{y4}} = \frac{1}{\left[\left(\frac{\pi}{A_4}\right)^2 - k_y^{\,2}\right]^{1/2}} \tag{2-16}$$

and

$$A_v = \frac{\pi}{\left(k_1^{\,2} - k_v^{\,2}\right)^{1/2}} = \frac{\lambda_o}{2\left(n_1^{\,2} - n_v^{\,2}\right)^{1/2}}, \qquad v = 2,3,4,5. \tag{2-17}$$

The transcendental Eqs. (2-11) and (2-12) cannot be solved exactly in closed form. One method, which can be used to solve this problem, is to assume that most of the power is confined in region 1. Hence,

$$\left(\frac{k_x A_{(3,5)}}{\pi}\right)^2 << 1 \text{ and } \left(\frac{k_y A_{(2,4)}}{\pi}\right)^2 << 1. \tag{2-18}$$

Therefore, the approximate solutions of (11) and (12) for k_x and k_y can be obtained by expanding the $\tan^{-1}$ functions in a power series.

2.3 EO Modulator

The search for a high speed optical or electro-optic (EO) modulator with low insertion loss and large optical bandwidth depends upon a workable architecture and the availability of a suitable EO material. The state-of-the-art in high speed modulators include the following:

- Magneto-Optic Modulators, which are relatively fast (< 1 GHz);
- Liquid Crystal (LC) SLMs, which are relatively fast and based on ferroelectric LCs with a 20 nsec maximum response time (equivalent to 50 MHz modulation frequency);

- Photorefractive Switches, which are based on $LiNbO_3$ (such as those produced by Crystal Technology, Inc.), or on PLZT (70 nsec response time);
- MQW modulators, which are super fast (> 1 psec);
- Plasmon modulators, which are extremely fast (> 5 psec); and
- Mach-Zehnder modulators, which are very fast (50 ps).

The successful fabrication of a high speed EO modulator depends upon the availability of a second-order EO polymer with high nanosecond susceptibility and the ability to maintain this susceptibility at high temperatures. EO polymers generally processed into thin films exhibit large nonresonant EO coefficients and low dielectric constants, from DC to multi-GHz frequencies. Recent advances in EO polymers include guest-host epoxies and polyimides exhibiting large EO coefficients at significantly higher temperatures than previously achieved. For the waveguide EO modulator fabrication, POC studied ROITech's polymers based on guest-host or polyimide structures.

In the Phase I project, POC investigated a multilayer EO modulator with a layer configuration similar to the surface plasmon modulator (SPM). This modulator has been tested for high speed modulation bandwidth, and its structure has proved to be viable for the proposed concept of UV-DOP technology.

Various fiber optic connectorization architectures were also studied. The initial studies were performed for four fiber optic modules; namely, an IC fiber module, a shipout line module, a 45° module, and a Y-junction module. The use of these modules in the UV-DOP technology provides flexibility in the PCB design, which is standard in all copper solutions.

3.0 WAVEGUIDE EO MODULATOR, BASIC DESIGN

3.1 Background

The unique system design is based on the generic idea of integrating singlemode Nonlinear Optical (NLO) channel waveguides with a thin film multilayer structure, combining dielectric claddings with thin film metallic layers (electrodes). This generic idea, patented by POC (see T. Jannson, et al., "High Modulation Rate Optical Plasmon Waveguide Modulator," U.S. Patent No. 5,067,788, November 26, 1991), is based on singlemode channel waveguide propagation perturbed by a metal-dielectric multilayer structure, represented by waveguide claddings and metallic electrodes. This statically perturbed channel waveguide propagation is additionally perturbed by the NLO electrooptic (EO) effect.

It is important to emphasize that although the system design is extremely complicated, the fabrication process is well established. It combines integrated optic channel waveguide fabrication with thin film multilayer fabrication of auxiliary structures (claddings and electrodes). We could say that the specifics of the fabrication process are analogous to those of IC fabrication. (Once the design and electronic layout is established, controlled, and well tested, the fabrication process is repeatable, with a high yield factor.)

The three major EO modulator topologies are: 1) NLO waveguide/phase modulators based on a single NLO channel waveguide; 2) Mach-Zehnder phase/amplitude modulators, based on a pair of channel waveguides (linear and nonlinear); and 3) POC's patented plasmon-amplitude modulator based on a simple linear channel waveguide and NLO cladding.

3.2 NLO-EO Effect Design Rules

Without poling, a $\chi^{(2)}$ polymer has an inversion symmetry that does not allow for the "linear" (Pockel) EO effect, also called the $\chi^{(2)}$ effect. In this case, the *index ellipsoid* has a fully symmetrical form. Linear poling, however, creates asymmetry for the eighteen (18) EO coefficients, emphasized by the r_{33} coefficient, and represented for the phase modulator by the so-called *half-wave voltage*, $V\pi$, in the form:

$$V\pi = \frac{\lambda}{2n_e^3\, r_{33}} \tag{3-1}$$

where n_e is the extraordinary refractive index, λ is the optical wavelength, and r_{33} is the electrooptic (EO) coefficient, satisfying the following relation for the NLO polymer:

$$r_{33} = 3r_{31} = 3r_{23} = 3r_{51} = 3r_{42} \tag{3-2}$$

For example, for $n_e = 1.6$, $\lambda = 1$ µm, and $r_{33} = 50$ pm/V, we obtain $V\pi = 2.4$ kV. It should be emphasized, however, that this auxiliary voltage is not real-voltage, which is applied transversally not longitudinally; thus, in order to obtain the real (applied) voltage, we need to reduce $V\pi$ by the waveguide width-to-length ratio, which for 3 µm width and 3 mm length is 1:1000. Therefore, the "true" transversal voltage is 2.4 kV:1000 = 2.4 V; i.e., very moderate.

3.3 Design Integration Software

A Design Integration Software (DIS) has been developed in this program for the generic design of the NLO/EO modulator. It consists of three basic software components:

A. Channel waveguide eigenstructure design
B. Multilayer cladding structure design
C. Perturbation calculus design

3.3.1 Channel Waveguide Design Integration Software (A)

The channel waveguide design integration software is based on a combination of the Effective Index Method with the Marcatili method. As a result, the singlemode condition is formulated for hybrid nodes $E^x_p y$, $E^y_p y$ (as described in the new textbook: Optical Interconnection, Foundations and Applications, ed. C. Tocci, H. J. Caulfield, Artech House (1994), p. 169, and co-authored by three of POC's scientists).

Example:

Consider a channel waveguide in the form of a raised step (see Figure 3-1), where $\lambda = 1.3$ µm, $n_f = 1.6$, $n_s = 1.55$. Then, the critical parameter, V_I, is

$$V_I = koT\sqrt{n_f^2 - n_s^2} = \frac{2\pi T}{\lambda}\sqrt{n_f^2 - n_s^2} = 2\pi x 0.4 x \frac{T}{\lambda} \tag{3-3}$$

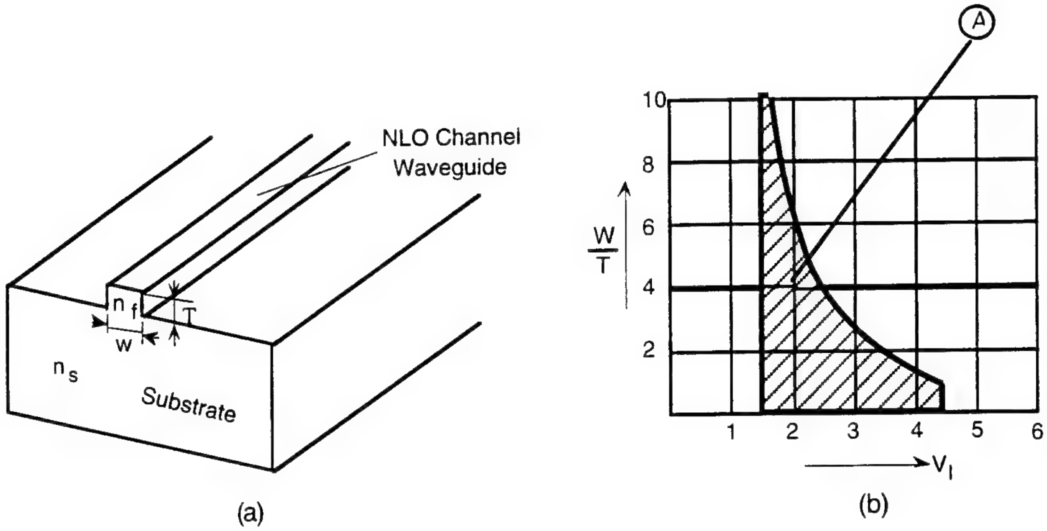


Figure 3-1
Illustration of singlemode condition for: (a) raised step channel waveguide; (b) The hatched area represents singlemode propagation. The point A has coordinates: $V_l = 2.5$ and W/T =2

From Figure 3-1(b), we select $V_I = 2.5$ in order to obtain well-confined singlemode propagation. Since $\lambda = 1.3$ µm, we obtain T = 1.3 µm. Then, we select the aspect ratio W/T=2 in order to obtain the well-confined singlemode propagation. Thus, W = 2.6 µm. The final structure is illustrated in Figure 3-2.

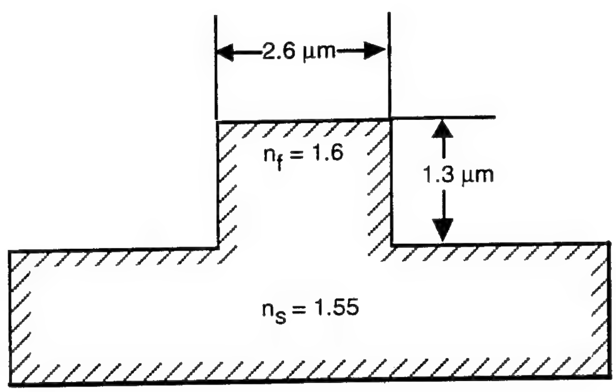


Figure 3-2
The Final Cross-Section Structure of a NLO Channel Waveguide, Designed by Optimized Procedure (A). As a result, the channel waveguide singlemode propagation is well-confined.

3.3.2 Multilayer Cladding Structure Design (B)

The upper metallic electrode structure integrated into a channel waveguide consists of a gap, a metallic layer (electrode), and a 5-layer thin film structure (Figure 3-3).

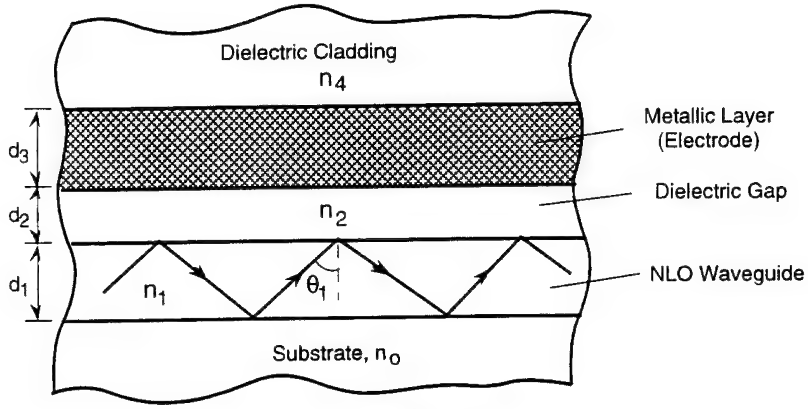


Figure 3-3
The upper electrode five-layer structure, including dielectric substrate (n_0), NLO waveguide (n_1, d_1), dielectric gap (n_2,d_2), metallic layer ($\hat{\varepsilon}_3$,d_3), and dielectric cladding (n_4)

The typical parameters for this structure are:

$$n_1 = 1.6,\ n_2 = 1.46,\ d_2 = 1.2\ \mu m$$
$$\hat{\varepsilon}_3 = -18 + i0.47\ \text{(silver)},\ d_3 = 500\text{Å} \tag{3-4}$$
$$n_4 = 1.46$$

The multilayer cladding structure design can provide the upper cladding structure in a sense of the complex reflectivity coefficient (Figure 3-4).

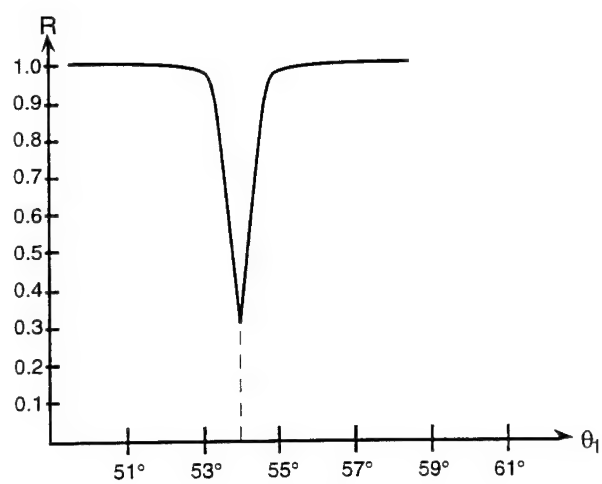


Figure 3-4
Typical (plasmon resonance-related) dependence of reflectance as a function of incidence angle, illustrated in Figure 3-2, for parameters defined by Eq. (3-4); $R = |\hat{r}|^2$, where $\hat{r} = \sqrt{R}\, e^{i\Phi}$ is the complex reflectivity coefficient.

3.3.3 Perturbation Calculus Design (C)

The complex reflectivity coefficient illustrated in Figure 3-3 is denoted as r_{1234}, in the form:

$$r_{1234} = \frac{r_{12} + h^2 r_{234}}{1 + r_{12} r_{234} h^2} \tag{3-5}$$

where

$$h = \exp(ik\xi_2 d_2) = \exp\left(-\frac{2\pi}{\lambda} d_2 |\xi_2|\right) \tag{3-6}$$

is the important gap coefficient, and for $\lambda = 0.63$ µm, and the parameter in Eq. (3-6) is: $h = 0.14$; also,

$$\xi_j = \left(n_j^2 - \beta^2\right)^{1/2} \tag{3-7}$$

where $n_j = \sqrt{\xi_j}$, and

$$\beta = n_1 \sin\theta_1 \tag{3-8}$$

is the *longitudinal wavenumber*, also called the *waveguide effective index*, while r_{12} is the Fresnel coefficient, and r_{234} is the compound Fresnel coefficient.

It was shown that in the thin gap approximation

$$h^2 \ll 1 \tag{3-9}$$

and that the *perturbed eigenstructure* is

$$\gamma_m = N_m^{(p)} + iK_m \tag{3-10}$$

where

$$N_m{}^{(p)} = N_m + \delta N_m \tag{3-11}$$

and

$$\delta N_m = -2\left(h^2/\chi\right) \sin 2\phi_{12} |r_{234}| \cos(2\phi_{234}) \tag{3-12}$$

$$K_m = 2\left(h^2/\chi\right) \sin 2\phi_{12} |r_{234}| \sin(2\phi_{234}) \tag{3-13}$$

where

$$r_{234} = |r_{234}| \exp(-i2\phi_{234}) \tag{3-14}$$

For an unperturbed waveguide:

$$\delta N_m = K_m = 0 \tag{3-15}$$

and

$$\gamma_m = N_m \tag{3-16}$$

where $N_m = \beta_m$ is the eigenvalue of the unperturbed waveguide.

In a similar way, we can calculate the lower electrode structure. The perturbation calculus is the basic method used to design an EO modulator as a combination of an unperturbed channel waveguide and a metal electrode cladding structure.

3.4 Waveguide/Modulator Fabrication Process

The Mach-Zehnder modulator is expected to be the simplest modulator that can be used in an integrated optical structure. ROITech's method of waveguide/modulator fabrication has been proven. ROITech uses a trench-and-fill waveguide process to build a Mach-Zehnder interferometer. The basic fabrication steps for a thin film waveguide device are:

- Start with a silicon substrate
- Deposit and pattern the base metal
- Coat the cladding layer and cure
- Photo pattern the waveguide trench
- Form the trench
- Coat the core material and cure
- Coat the top cladding layer and cure
- Deposit and pattern the top metal
- Align the NLO material with an electric field
- Test the wafer
- Dice

These steps are schematically illustrated in Figures 3-5 (a) and (b). To make a practical device for optical interconnects, several additional circuit elements are required. Electrical vias are required for the interconnection of the base metal with the top surface. In-plane mirrors enable the design and fabrication of a compact circuit by the use of 90° bends in the waveguide. Out of plane mirrors and integrated lenses allow a simplified hybrid planar assembly process and a smaller overall package size. These via and mirror structures require additional processing steps to be added to the basic process outline. The additional steps impose further requirements on the multilayer processing capability of the materials.

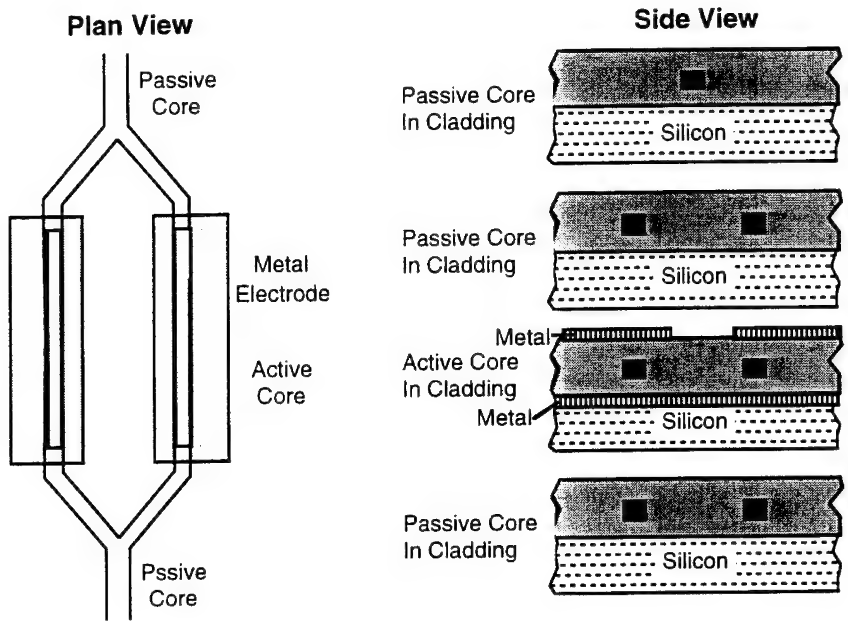


Figure 3-5(a)
Hybrid Active/Passive Waveguide Modulator, Following ROITech's Design

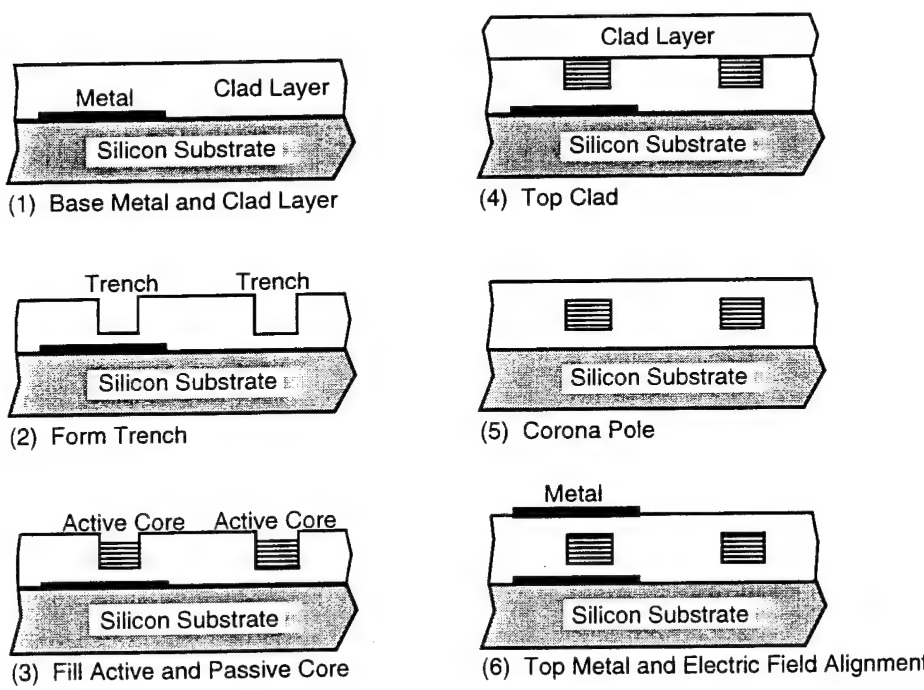


Figure 3-5(b)
Optical Integrated Circuit Hybrid Waveguide Fabrication Sequence, Following ROITech's Design

The full optical integrated circuit (OIC) process sequence that has been developed by ROITech follows:

- Start with a silicon substrate
- Deposit and pattern the base metal
- Coat the cladding layer and cure
- Photo pattern the waveguide trench
- Form the trench and out-of-plane mirror
- Metallize and pattern the out-of-plane mirror
- Coat the active and passive core materials and cure (hybrid waveguides)
- Coat the top cladding layer and cure
- Pattern and form the in-plane mirror and electrical via
- Metallize and pattern the via and in-plane mirror
- Fill the mirror structure
- Deposit and pattern the top metal
- Align the NLO material with an electric field
- Test the wafer
- Dice

The full process is more extensive than the simple test process, and imposes further requirements on the material system. This multilayer process sequence requires multiple coating and curing steps that must not damage the lower material layers. The active core material must be robust enough to allow the subsequent processing of two additional polymer layers, as well as two metallization and patterning steps. This process sequence enables the fabrication of compact OICs for assembly into a hybrid integrated optical circuit (HIOC) using UV-DOP technology. The specific design parameters, such as waveguide dimensions, separation, modulator arm length, etc., can be accommodated in ROITech's fabrication process.

3.5 Material Issues

3.5.1 ROITech-Designed EO Chromophores

According to laser optronics, there are a large number of organic materials (60,000) from which a NLO material can be readily synthesized. Since no one knows which will be the best for any given application, research and development in material synthesis and testing continues. In our Phase I investigation, we studied ROITech's RT-9800/PQ-100 guest host material and University of Southern California's PUR-DR 19 material for the possible inclusion in the modulator system. ROITech's earlier results demonstrate that the use of heteroaromatics as conjugating moieties strongly enhances the molecular hyperpolarizability ($\beta\mu$) of the charge transfer compounds. ROITech's researchers have made numerous classes of molecules with excellent optical nonlinearity ($\beta\mu$ value as high as $10{,}000 \times 10^{-48}$ esu at 1.9 μm). A partial list of these NLO chromophores is shown in Table 3-1. The broad range of absorption spectra and very high nonlinearity achieved by employing heteroaromatics as conjugating moieties coupled with various efficient electron donors and acceptors clearly provides a vast array of potential molecules.

In addition to these primary nonlinear optical properties, ideal chromophores should also possess several desirable secondary properties, including:

1. High intrinsic thermal stability;
2. Chemical resistance toward processing solvents and polymeric materials at elevated temperatures;
3. Photochemical stability;
4. Hydrolytic stability; and

5. Compatibility with the polymer matrix.

Table 3-1. Examples of ROITech Designed EO Chromophores

Compounds	λ Max (nm)	($\beta\mu$ x 10^{-48} esu)
DANS	424	580
ENO-4301	514	2100
ENO-2P02	571	2200
ENO-3203	547	2300
ENO-1105	638	2400
ENO-2111	578	2400
ENO-2208	585	2600
ENO-1118	651	2600
ENO-3304	622	2600
ENO-2217	613	2700
ENO-2114	545	2700
ENO-2117	608	2800
ENO-1120	736	3100
ENO-2216	638	3300
ENO-2211	664	3500
ENO-2P03	638	3500
ENO-4302	556	3800
ENO-2213	665	3800
ENO-2113	597	4200
ENO-3303	593	4300
ENO-2108	640	6200
ENO-2214	680	6700
ENO-2212	718	6900
ENO-3205	653	7300
ENO-2116	662	9100

Having achieved a major success in primary nonlinear optical properties, ROITech has focused its research on obtaining suitable secondary properties. A unique approach was developed to enhance thermal and photochemical stability of chromophores without sacrificing optical nonlinearity. Functionalized heteroaromatic conjugated compounds without p-bridges, such as fused-ring or single-ring heteroaromatics, possess high thermal stability (> 300°C) and are photochemically stable to visible light. The achievement of intrinsic thermal and photochemical stability, however, is not sufficient to ensure high temperature stability in a polymer matrix. Many high temperature matrices (such as polyimides) are very reactive toward the chromophores, particularly during the imidization step. Therefore, the chemical stability of the chromophores in the reactive environment of the polymer matrix is a crucial requirement.

Intensive research efforts have also been directed at developing suitable electron-donors and electron-acceptors with chemical resistance (to, e.g., processing solvents, acidic and basic environments of polymers) at elevated temperatures.

Based on these chromophore developments, a highly nonlinear optical active dye ($\beta\mu$ = 6,200 x 10^{-48} esu) has been incorporated at 20 wt.% in a high temperature polyimide (Tg = 265°C). The electrooptic coefficients (r_{33}) measured at 1.3 µm ranged from 25-35 pm/V, depending on the poling field strength. Most importantly, the EO signal of the poled sample remains very stable in a heated oven at 100° C for a long period of time (months). This result clearly demonstrates two advantages of using these NLO chromophores in high temperature polymers: high electrooptical properties and high thermal stability.

3.5.2 RT-9800/PQ-100 Guest-Host EO Polymer

The five-membered heteroaromatic rings form a conjugated structure that strongly enhances the first order optical hyper-polarizability (B). The structure of the heteroaromatic *chromophore diethyl-amino-tricynovinyl substituted cinnamyl thiophene (RT-9899)* employed in this work is reported earlier. This compound demonstrates exceptionally large second order nonlinearity. The $\mu\beta$ value (9800 x 10^{-48} esu) (the product of molecular dipole moment and microscopic second order susceptibility of this compound) was measured out at 1.907 µm using an electric field-induced second harmonic generation (EFISH). This is approximately 15 times larger than that of diethylamino-nitrostibene (DANS), which is a commonly used chromophore in second order nonlinear optical material development.

Polyquinolines are ideal polymer materials for device fabrication, because they are mechanically strong, easily processed into low optical loss thin films, and thermally stable up to 500 – 600° C. The polyquinoline (PQ-100) used in this work was purchased from Maxdem. Polyquinolines are very soluble in common organic solvents, such as cyclopentanone, NMP, DMAC, etc. The polymer solution can be easily spin-coated onto substrates such as glass and silicon wafers to form thin films. The chromophore RT-9800 is readily dissolved in the polyquinoline/cyclopentanone solution at a 20% by weight content of the chromophore relative to the polyquinoline. Further increases of the weight fraction of the chromophore may result in aggregation of the dye. Very good quality thin films (2-4 µm) were obtained by careful spin-coating of the filtered (through a 0.2 µm microfilter) polymer solution onto an indium tin oxide (ITO) coated glass substrate. After being soft baked at 110° C to remove residual solvent, a thin layer of gold was deposited onto the film by sputtering (Desk II, Denton Vacuum). The original glass transition temperature (Tg) of PQ-100 is 265° C; however, after being doped with 20 wt% of RT-9800, the Tg dropped to ~180°C due to plasticization. The film was poled at 180°C for 5 minutes in Argon with an applied electric field of around 0.8 MV/cm. The poling field was removed after the chromophore/polyquinoline film was slowly cooled to room temperature.

The EO response of the poled RT-9800/polyquinoline film was measured using an ellipsometric technique. In order to minimize the contribution due to resonant enhancement, the EO coefficient (r_{33}) was measured at a wavelength of 1.3 µm. For a 20 wt % RT-9800/polyquinoline film poled at 0.8 MV/cm, an r_{33} value of 45 pm/V was achieved. This nonresonant r_{33} value was not only much larger than most of the organic and polymeric nonlinear optical materials, but also exceeds that of $LiNbO_3$. The standard inorganic EO coefficient can be expected if the processing environment can be further improved.

The experimental value of r_{33} agrees fairly well with the predicted value of 48 pm/V calculated from mb using a two-level model suggested by Singer et al., after accounting for dispersion effects from both the EFISH and EO measurements.

3.5.3 EO Polymer with Side Chain Polyimides for High Temperature Applications

Most of the results reported in literature for high temperature NLO polymers are centered around the guest/host approach. Although this approach offers the convenience of simply dissolving NLO chromophores (in polyamic acids/polyimides), there are several severe deficiencies, including:

- Low loading level (solubility of dyes in processing solvents and polymer matrices)
- High optical loss (due to dye aggregates)
- Low compatibility (dye sublimation or aggregation)
- Low Tg (due to the plasticization of NLO dyes)

Earlier results from literature prove that side-chain acrylate NLO polymers possess several advantages over guest/host systems, such as:

- Higher loading levels
- Better optical quality
- Better alignment stability for the EO signal
- Higher EO coefficients due to the liquid-crystalline effect of the side chains

However, the functionalization of very reactive diamine and dianhydride monomers required for polyimides is considerably more difficult than for acrylate systems. ROITech has some innovative approaches to easily synthesize NLO side-chain polyimides. Preliminary results demonstrate high r_{33} values (10-20 pm/V), good film forming properties, high loading level of dyes, and no sublimation of the dye at high temperatures.

Through the selection of various aromatic diamines and dianhydrides, ROITech has been able to fine-tune several critical polymer properties, such as Tg, solubility, and mechanical properties. The poled polymers exhibit temporal stability for an extended period of time at 110° C. Higher thermal stability can be achieved through the incorporation of "double-ended" functional groups, as was pioneered by Professor Larry Dalton at USC. The side-chain polyimide can be hardened by this crosslinking mechanism during the poling process to enhance the poled thermal stability. Also, the EO activity can be enhanced by incorporating dyes with higher hyperpolarizability.

3.6 Study of the IC Die Bonding Techniques

An investigation of bonding techniques was important to determine the packaging requirements for the modulator.

Two major bonding methods are used to attach bare silicon dies to a substrate: 1) epoxy adhesives; and 2) solder or alloy attachment. A comparison between these two methods is shown in Table 3-2. From Table 3-3, we can conclude that polyimide adhesives exhibit

high thermal stability; however, epoxies are a better, more cost-effective solution for temperatures lower than 1

Two types of epoxies are used for die assembly: 1) electrically conductive; and 2) electrically non-conductive. The first one is used for attaching transistors, ICs, and capacitors to substrates, and the second to attach substrates to packages. A summary of the electrical properties of electrically conductive and electrically insulative adhesives for die and substrate attachment is shown in Table 3-2, where the most attractive methods of attaching IC dies to substrates are described.

There are several methods of attaching IC dies to substrates. The most popular are:

- Wire bond
- Tab (face-up)
- Flip tab (face-down)
- Flip-chip
- Microbumps

Wire bonding is still one of the most popular techniques; however, emerging new technologies such as TAB bonding, ribbon bonding, flip-chip bonding, overlay batch metallization, and anisotropic adhesive bonding are becoming more popular and cost effective, especially in producing short interconnect paths and high packaging densities. A summary of different die bonding techniques is shown in Table 3-3 while a comparison of the characteristics of the different techniques is given in Table 3-4. For the development of the UV-DOP technology, we have selected polymer flip-chip solderless bonding technology. The detailed description of this technology will follow.

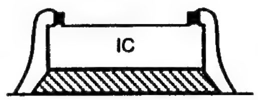
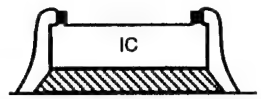
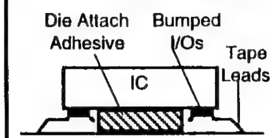
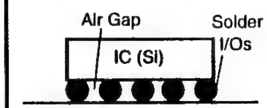
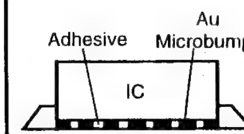
Table 3-2. Comparison of Bonding Techniques

Epoxy Advantages	Solder or Alloy Advantages
Low processing temperatures (150 to 180° C cure).	High thermal conductivity, best approach for high-power circuits.
Low-cost batch processing (screen printing, stamping, or automated dispensing) available in paste, tape, or perform.	Available as performs.
Ease of rework, softens under temperature and pressure.	No outgassing circuits meet class K, low H_2O requirement $\leq$ 3000 ppm.
Available in both electrically conductive and insulative versions.	High processing temperatures; 300° C can degrade wire bonds and devices.
Risk of excessive outgassing (H_2O, NH_3, etc.).	Limited rework due to higher solder melt temperatures.
Risk of excessive contaminants (Cl^-, F^-, Na^+).	Risk of metal particle generation or splatter.
Risk of particle generation.	Only available in electrically conductive version.
Possible interface resistance increase.	
Cleanliness control for best adhesion.	
Poor to moderate thermal conductivity.	

Table 3-3. Electrical Properties of Conductive and Insulative Adhesives for Die Attachment

	Resin	Filler	Form	Volume Resistivity, gxcm	Thermal Conductivity W/(mxK)	(Tg) °C	CTE+ (ppm/°C)
Conductive Adhesives	Epoxy	Silver	Paste	1×10^{-4}	1.87 - 3.0	126	46
				7×10^{-5}			
	Epoxy	Gold	Paste	8×10^{-4}	1.7 - 2.0	69-107	50-57
	Epoxy	Copper	Paste	2×10^{-3}	1.38	59	46
	Epoxy	Silver	Film	2×10^{-4}	1.0 - 2.1	81	66
Insulative Adhesives	Epoxy	None	Paste	4×10^{14}	0.2 - 0.7	130	35
				3×10^{15}			
	Epoxy	Alumina	Paste	$1\text{-}4 \times 10^{12}$	0.52 - 1.42	85	41
	Epoxy	Diamond	Paste	10^{14}	11.6	-25	120
	Epoxy	Diamond	Film	$> 10^{14}$	11.6	-25	110
	Epoxy	Glass Fabric	Film	7×10^{12}	0.27 - 1.12	102 - 140	50 -83
				8×10^{14}			

Table 3-4. Five Major Die Bonding Techniques Characterization

	Wire Bond	TAB (Face-Up)	Flip TAB (Face-Down)	Flip-Chip	Microbumps
					
Substrate metallization	Non critical: thin- or thick-film gold	Not critical Au or solder	Not critical: Au or solder	Low CTE (1) Si on AlN required for large chips (> 170 mils) Solder bond pads (size critical)	CTE less critical Planarity critical
Interconnect	Gold or Al wire	Au weld on solder Cu tape leads (Au plated/ welded or soldered)	Au weld or solder Cu tape leads (Au plate/ welded or soldered)	Solder	Metal contact (pressure), adhesive bond
Bonding process	Thermocompression, Thermosonic, ultrasonic	Chip-specific tape TAB ILB (2)/AB (3) gang or single-point	Chip-specific tape, TAB ILB/OLB; gang or single-point	Solder reflow (batch) Heat, inert atmosphere	UV cure under high pressure (6000 - 12,000 kg/cm^2
Die attachment	Conductive/ nonconductive adhesive or metallurgical	Conductive/ nonconductive adhesive	Nonconductive adhesive or no adhesive	Nonconductive adhesive or no adhesive	UV cured acrylic resin
I/O pitch (min) I/O location	6 mils proved Staggered	4-8 mils Perimeter	4-8 mils Perimeter	8 mils Perimeter or area	10 mm (0.4 mil) Perimeter (or area with transparent substrate)
Reworkability	Yes	OLB-yes	OLB-yes	Difficult (solder volume control oxidation without flux)	Unknown
Die-to-die	50-70 mils	100 mils standard, 70 mils feasible	70-180 mils feasible	10-30 mils feasible (rework limited)	Unknown
Reliability issues	Reliability proven Nondestructive Pull testing	Visual inspection possible Bond integrity being addressed	Visual inspection possible Bond integrity being addressed	Inspection difficult CTE matched substrate required to reduce solder fatigue Difficult to clean beneath die	Inspection extremely difficult Limited temp. tests look OK; long-term tests and RGA unknown
Electrical	Speed and power limited	Low inductance, resistance	High speed performance may be affected by adhesive	Best peformance	High speed performance may be affected by adhesive
Heat dissipation	Best for metallurgical attachment	Good through adhesive and Cu leads	Good through adhesive and Cu leads	Poor through solder I/Os (depends on total I/O area)	Very good through microbumps and very thin adhesive (3 mm)
Technological maturity	Very mature	Demonstrated by many, most applications single-chip, high volume	Demonstrated with air gap under chip; 8-mil pitch, solder/Au OLB	Demonstrated in production: IBM Delco, Motorola (8-mil pitch, min.)	Demonstrated 10 mm pitch (Matsushita)
Key issues	Device pretesting at speed difficult	IC bumping required Tape, hand tooling required for each IC type Tape quality/delivery delays Burn-in	IC bumping required Tape, hand tooling required for each IC type Tape quality/delivery delays Burn-in	Device pretesting, heat dissipation, inspectability, rework IC bumping required	Device pretest, incompatibility with nonplanar substrates. Nonstandard IC microbumping, special processing equipment (heat pressure, leveling, UV cure)

(1) CTE - coefficient and thermal expansion (2) ILB - Inner-lead bonding (3) OLB outer-lead bonding

3.6.1 Solderless Flip Chip Technology

In Phase I, we also studied a new solderless flip-chip technology. This technology can help mount all of the dies on the silicon substrate. It involves the deposition of a low dielectric constant organic polymer onto the silicon die in wafer form, leaving the bond pads open. This is accomplished using Advanced Wafer Passivation (AWP), which employs high precision automatic screen printers with pattern recognition alignment. Subsequently, an electrically conductive polymer is stenciled onto the bond pads of each die of the wafer to form the solderless bumps, and is then cured. Silicon nitride is the passivation coating chosen for the wafers.

In the first step, shown in Figure 3-6(a), a 25 μm layer of dielectric polymer is screen printed over the entire surface of the wafer, excluding the bond pads and streets. This is accomplished using a high precision screen printer. This is essential as a secondary protective layer, and more importantly, for the formation of the "dam" around the bond pads, which restricts the flow of conductive material and prevents bridging between adjacent bumps. The bond pads are aluminum, 100 μm on a side, and the spacing between bond pads is 200 μm. The dielectric is usually cured in 12 minutes via an N_2 purged IR tunnel using a four-step heating profile.

The next step in the process (shown in Figure 3-6(b)) is the stencil deposition of the conductive polymer into the wells surrounding the bond pads. The bond pads are covered, and the height of the deposit is close to 25 μm. This represents the first layer of the conductive bump, which is cured in the IR, and serves as the foundation for the conductive polymer bumps. An open stencil is used in place of a screen to ensure that the conductive polymer is pushed into the 25 μm deep via and makes good electrical and mechanical contact with the A1 bond pads.

Having provided a foundation of conductive polymer, the flip-chip assembly is ready for the application of the conductive bump, as shown in Figure 3-6(c). Using the same stencil, the wafer is aligned to the stencil and the conductive polymer bumps are deposited on top of the first layer of conductor. The deposition height is again 25 μm. This can be varied between 15 and 50 μm. The conductive bumps are cured in the N_2 purged IR tunnel, and at this stage the flip-chip assemblies are now completed.

The completed flip-chip wafers with the cured dielectric coating and conductive bumps are then diced into individual flip-chips and substrates. The next step is the actual mounting of the flip-chip onto the substrates for completion of the flip chip assembly. A 2 mil layer of conductive polymer is stenciled onto the bond pads of the substrate, and the flip-chip is aligned and mounted onto the substrate, as shown in Figure 3-6(d). The bumps of the flip-chip are connected to the wet adhesive on the corresponding bond pads. 300X magnification is used to ensure accurate alignment of the flip-chip. The fixturing of the flip-chip is completed by curing it for 10 minutes at 50° C on the heated stage of the flip-chip aligner/bonder.

The completed flip-chip assembly, as seen in Figure 3-6(e), can be tested for electrical continuity and mechanical integrity. Die shear testing can be performed in accordance with MIL-STD-883C, Method 2019, using an "HMP" die shear tester. Shear strength data shows no loss of adhesion of the polymer bumps when subjected to 10 kg shear forces.

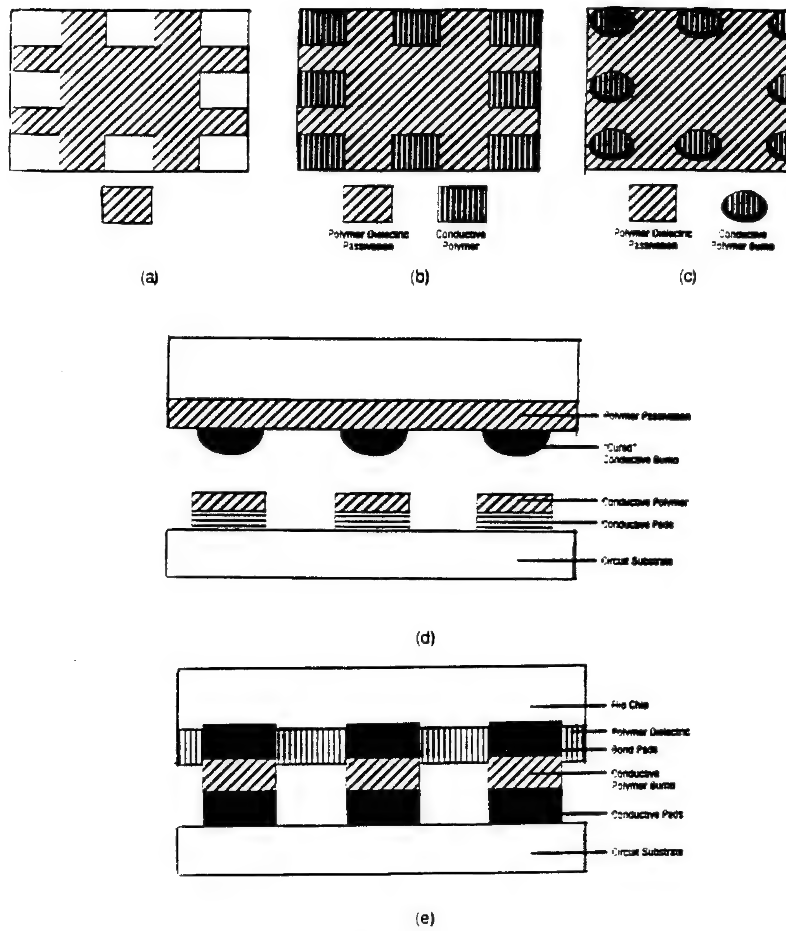


Figure 3-6
Polymer Flip Chip Bonding Steps Applied for the UV-DOP. (a) Dielectric polymer; (b) Fabrication of conductive polymer bumps; (c) Foundation of conductive polymer bumps; (d) Side view of the flip; and (e) Final assembly.

Assembled flip-chip devices are conformally coated with a "glob-top" adhesive and environmental testing is conducted at the end of the fabrication process. The coating protects the bump interconnects and the silver epoxy from any potential problems with Ag migration induced by moisture and current flow. These devices are usually subjected to 1,000 hr THB (85 percent RH: 85°C) testing and thermal cycling.

3.6.2 Advantages of Solderless Flip-Chip Technology

The process development matrix discussed in this report confirms the feasibility of manufacturing solderless flip-chip assemblies. The results show that the AWP approach to forming conductive polymer bumps offers several advantages for flip-chip microcircuit fabrication. These include: straightforward screen printing, low temperature processing of organic materials, elimination of cracking problems, low-cost operations, and others.

3.7 Integrated Optic Data Channels

For system level application of the EO modulator, it is critical to integrate channel waveguides and modulators with the chip substrate. In recent years, the fabrication of channel and planar waveguides has been reported on various substrate materials, including GaAs, Si, $LiNbO_3$, glass, and printed circuit boards. Different fabrication methods are applied, depending on the substrate material used. For example, waveguides can be fabricated on GaAs with $GaAs/Ga_xAl_xAs$ heterostructure layers using metal oxide chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), or liquid phase epitaxy (LPE) growth techniques. Channel waveguides can be realized by chemical or reactive ion etching. On a Si substrate, a SiO_2-TiO_2 waveguide layer can be fabricated using a flame hydrolysis deposition method. On $LiNbO_3$ and glass waveguides, channel and planar waveguides can be fabricated using ion exchange.

Several different substrate materials, including conductors, semiconductors, insulators, and ceramics can be coated this way. Polymer waveguides are compatible with the solderless flip-chip technology, due to its low temperature processing requirements.

3.7.1 Fiber-to-Waveguide Coupling Method

The advantages of the grating coupling method are: high efficiency, selective mode excitement, compactness, and easy adjustment. The 1st and 2nd layers of fabrication are also described in detail. The summary of this technologic approach is shown in Figure 3-7.

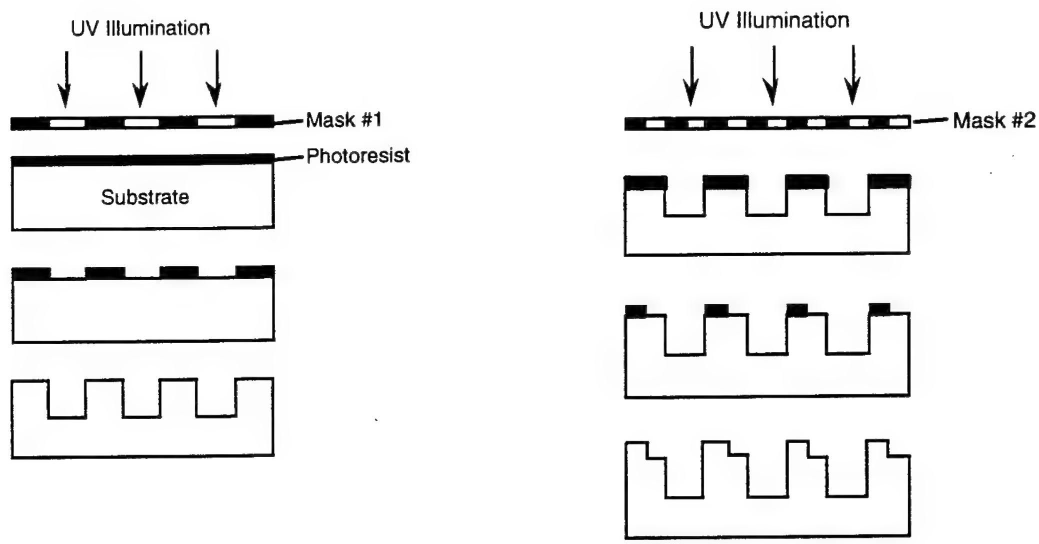


Figure 3-7
Summary of Technologic Approach for Lithographic Fabrication of Grating Couplers.

4.0 POTENTIAL POST APPLICATIONS

The high-density 2D packaging and interconnection schemes for the new generation of ICs proposed here can be employed in DOD electronic systems to reduce their size and weight, and to drastically improve the speed of Very Large Scale Integration (VLSI), Application-

Specific Integrated Circuits (ASIC), and Very High Speed Integrated Circuit (VHSIC) multichip modules. They can improve the reliability of compactly packaged systems against radiation loss and electromagnetic interference. An improvement in system thermal performance can also be expected because of the reduced use of electrical interconnects, and thus reduced power consumption (used only to connect chip outputs with modulators and detectors). This compact 2D packaged system will be suitable for military applications. For example, it can be used in high speed and reliable processors employed for rapid target recognition and missile interception. It can also be used to protect other military electronic systems against EMI-related electronic jamming. Civilian applications include forming high-speed multi processor systems for medical image processing, data fusion, neural computing, and the construction of a new generation of high speed 2D packaged optoelectronic computers or workstations. Applications in high-speed electronic instruments is a commercial goal. With this interconnect technique, computing speeds can exceed several hundred MHz. The proposed UV-DOP technology scheme will improve the performance and reduce the cost of high speed electronic instruments such as signal generators, oscilloscopes, network analyzers, and computers. Space programs can also benefit from the resulting dimension and weight reductions, greater reliability, better system redundancy, and radiation-hard performance.

4.1 Potential Commercial Components

The component applications of the EO modulator technology resulting from this program addresses the fast growing SONET OC-24 and OC-48 network markets. This is a potentially progressive market, since it will be a standard interface interconnect in the near future (less than 2 years) for ATM (Asynchronous Transfer Mode) applications. The current limitation on the wide use of high speed (> 1Gb/s) electrooptic components (based on $LiNbO_3$ produced by AT&T, UT-Photonics, E-TEK, and others) is their high cost (a few thousands dollars). The proposed polymer-based EO modulator can potentially result in low-cost modulator devices (below $200). The market value can be estimated as > $100M, based on the estimated $5B SONET market in by the year 2000.

The array packaging of transmitters (E-to-O) and receivers (O-to-E) can also result in parallel data links for computer-to-computer and video communications, which require a large number of high bandwidth data channels. Presently, parallel transmitters and receivers have been developed by Motorola Inc. with 10 parallel channels and total data speeds of 3Gb/s (see Electronic Design, November 21, 1994). POC also views this parallel link as an important communication product component. Recently, we have developed a transmitter array containing four lasers and four fibers. POC is committed to this type of product development, and views this proposed program as an important vehicle in realizing a new generation of parallel links using low cost polymer-based plasmon EO modulators.

4.2 Government Applications

Government applications include broadband computer interconnects, Command and Control (C^2) data distribution and data fusion, high-noise HD sensor imagery (which cannot tolerate image compression), multimode information systems and data buses, HD video distribution for training and distance learning, rapid force deployment, video assisted logistics and maintenance, and interactive video for command centers. The Navy's massive COPERNICUS command and control architecture integrating satellite (INMARSAT) communications, radar baseband signal distribution, processing, and many

others will benefit from the application of ultra high speed optical fiber networks using surface plasmon waveguide modulators. Other applications are global grid (GG) and theater extension network (TENet), which provide an extension of DOD, and which require multi-Gbit/s data rate transmissions.

4.3 Technology Transition for System Application

For the first time (and at modest cost), the highly interconnected multiprocessor systems will enable highly complex simulations and calculations, including parameter optimization in a very large data space of $\sim(10^4)^3$ points, decision making based on a large neural network with $\sim 10^6$ input neurons, the modeling of *drag coefficients* of aircraft and missiles, the design of high-speed integrated circuits (IC) and highly dense multi-chip modules (MCMs) for the *next generation in electronics,* the classification of *plume and radar signatures,* and the simulation of bimolecular reactions for new drug development and optimization, to mention just a few.

The increasing demand for very high-speed computations has resulted in the development of powerful computers, able to handle billions of operations per second (BOPS). Both single CPU supercomputers and multiple processor systems have been promoted to dominate the high speed computing market. Recently, a significant amount of research has been devoted to the development of parallel computers, which will eventually dominate both the commercial and military markets, and offer tens of giga floating operations per second (GFLOPS) speed. Parallel computers, such as the *Touchstone Delta,* the *Kendall Square* (KSR), and the *Connection Machine II* belong to the new generation of American-made parallel computers. There is also growing competition from abroad, especially from Japanese companies such as NEC, Matsushita Electric Industrial Co., Ltd., and Media Research Holotronics. Two prime Japanese parallel computers are the *Word Scalable Parallel Machine* with a 12.8 GLOPS peak processing power, developed by NEC Corp. (June 1993), and Matsushita's *Alternating Direction Edition Nexus Array System,* which is a parallel computer with up to 1024 processing elements. As good as these machines are, however, more research is needed to improve their performance and lower their cost. American leadership in the 21st century computer market will depend on how effectively we can develop innovative lower cost systems with thousands of parallel processing elements capable of communicating without major bandwidth limitations. The proposed UV-DOP technology will play a significant role in these system development efforts.

5.0 CONCLUSIONS

In summary, POC made the following findings in this Phase I program:

1. The electrooptic polymer can be synthesized as a stable material for the development of the EO modulator.

2. The EO polymers from ROITech and the University of Southern California (USC) meet the EO modulator design and fabrication requirements.

3. Both polymers can retain their EO coefficient at 90 °C without any significant degradation or loss in EO coefficient.

4. An EO modulator based on either the ROITech's or USC's nonlinear optical polymers can be integrated into an ultra-high density optical packaging system using solderless bonding and flip-chip technology.

5. An enormous application potential exists for both the EO modulator as an individual component and as a high density chip packaging technology for the communications industry.

6. Software developed in this Phase I program has been very helpful in the design and optimization of channel waveguides including arrays of waveguides embedded in multilayer structures. This is of great importance in the design and interpretation of EO modulators and channel waveguides, both essential to this program.

6.0 RECOMMENDATIONS

Based on the successful results of the Phase I program, POC is pleased to make the following recommendations for continued work in Phase II:

1. Further investigation of the EO materials and EO modulator is needed to optimize the design of the ultra-virtual density optical packaging technology so that it can be used to many dual-use applications.

2. Optimize the waveguide structure to minimize insertion and absorption loss, and crosstalk loss.

3. Study the issues related to the integration of this technology with standard IC Dies waveguide modulator. This is necessary to insure the reliability and repeatability of this ultra-virtual density optical packaging technology.

4. Investigate the waveguide-to-fiber coupling so that a connectorization scheme can be chosen.

5. Further the development of the Design Integration software (DIS), provide documentation, and perform debugging to optimize the multilayer fabrication of the high density packaging system.

6. Further optimize the waveguide design software by providing a variety of materials for substrate and cladding. Enable optimization of curved waveguides as well as "y" junctions for fan out operations.

APPENDIX A

ABOUT THIS PROGRAM

The program for channel waveguide design and optimization is written in MATLAB, which provides graph function, 1D, 2D, and 3D, for the computer simulated data.

1. Program Teeigen gives the simulation for dielectric channel waveguide, such as field profile of the modes, dimension for single-mode operation, effective index, and so on.

2. Program Tmeigen gives the simulation for channel waveguide with one metal cladding layer.

3. Program TANG is a modified program for program Teeigen, which gives the effective index Vs channel width.

To run the program, simply open file TANG, for example, in your Macintosh as you open any file. Then, go to the command file on the same screen as you usually do with Macintosh . Type TANG in the command file, and you will see the plot of the effective index Vs channel width.

```
function [root,flag] = bisect(nstart,nlast,th)

% The interval in which the root is required to be found is
% given by nstart= (n1 or n3) depending on whichever is higher.
% and nlast= n2.

first=nstart;
last=nlast;

% The values of the eigenvalue equation is found for the above
% two values of n.

temp1=dispersion(first,th);
temp2=dispersion(last,th);

% The algorithm to find the optimum root
flag = 0;
if temp1*temp2<0.0,
   while (abs(temp1-temp2)>1.0e-3)
          middle=(first+last)/2;
          temp3=dispersion(middle,th);
          if temp3*temp1<0.0,
             last=middle;
             temp2=temp3;
          elseif temp1*temp3>0.0,
             first=middle;
             temp1=temp3;
          end
    end
    root=middle;
else
    flag = 1;
end
```

```
function[value] = dispersion(neff,t)

% Wavelength of the light source in free space
lambda = 633e-9;
im = sqrt(-1);
k = 2*pi/lambda;

% Thickness of the slab
%t = 0.5e-6;

% Refractive indices of the supersubstrate, core and the
% substrate respectively.
n1 = 1.5;
n2 = 1.52;
n3 = 1;

% permittivities of the meidum
e0 = 8.85e-12;
e1 = (n1^2)*e0;
e2 = (n2^2)*e0;
e3 = (n3^2)*e0;
eeff = (neff^2)*e0;

% normalized frequency parameter
v = k*t*sqrt((e2-e3)/e0);

% Normalized b parameter
b = (eeff - e3)/(e2-e3);
if b == 1
   b1 = inf;
else
   b1 = 1.0/(1-b);
end

% Asymmetry measure for TE modes
a = (e3-e1)/(e2-e3);

% Eigen equation for TE modes
value = m*pi + atan(sqrt(b*b1)) + atan(sqrt((b+a)*b1)) - v*sqrt(1-b);
```

```
global m

% Initial parameters
im = sqrt(-1);
c = 3.0e+8;
n1 = 1.5;
n2 = 1.52;
n3 = 1;
lambda = 633e-9;
omega = c/lambda;
k = 2*pi/lambda;
mu = 1.2555e-6;

ti=0.5e-6;
m = 0;
for i = 1:10
    thick(i) = ti;
    height = ti;
    [alpha,pointer] = bisect(n3,n2,height);
    solution(i) = alpha;
    ti=ti+0.5e-6;
end

plot(thick,solution)
```

```
global m

% Initial parameters
im = sqrt(-1);
c = 3.0e+8;
n1 = 1.5;
n2 = 1.52;
n3 = 1;
t = 0.5e-6;
lambda = 633e-9;
omega = c/lambda;
k = 2*pi/lambda;
mu = 1.2555e-6;

% mode number
m = 0;
[alpha,pointer] = bisect(n3,n2);

while pointer == 0
      solution(m+1) = alpha;
      m = m + 1;
      [alpha,pointer] = bisect(n3,n2);
end

for i = 1:m
    q(i) = k*((solution(i)^2 - n1)^0.5);
    h(i) = k*((n2^2 - solution(i)^2)^0.5);
    p(i) = k*((solution(i)^2 - n3^2)^0.5);
    beta(i) = k*solution(i);
    den = beta(i)*(t+(1/q(i))+(1/p(i)))*(h(i)^2+q(i)^2);
    cons(i) = 2*h(i)*sqrt(omega*mu/den);
end

pts=200;
for i = 1:m
  for j = 1:pts
    if j == 1
       x(j) = -1.25*t;
    else
       x(j) = x(j-1) + 2.5*t/pts;
    end
    if x(j) < -t,
      inter = cons(i)*(cos(h(i)*t)+(q(i)/h(i))*(sin(h(i)*t)));
      field(i,j) = inter * exp(p(i)*(x(j)+t));
    elseif  (x(j) >= -t)  & (x(j) <= 0),
```

```
      inter = cos(h(i)*x(j))-(q(i)/h(i))*sin(h(i)*x(j));
      field(i,j) = cons(i)*inter;
    else
      field(i,j) = cons(i) * exp(-q(i)*x(j));
    end
  end
end

plot(x,field)
```

```
function [root,flag] = bisectmet(nstart,nlast,nlow,length,in)

% The interval in which the root is required to be found is
% given by nstart= (n1 or n3) depending on whichever is higher.
% and nlast= n2.

first=nstart;
last=nlast;

% The values of the eigenvalue equation is found for the above
% two values of n.

temp1=dismetal(first,length,nstart,nlast,nlow,in);
temp2=dismetal(last,length,nstart,nlast,nlow,in);

% The algorithm to find the optimum root
flag = 0;
if temp1*temp2<0.0,
   while (abs(temp1-temp2)>1.0e-4)
          middle=(first+last)/2;
          temp3=dismetal(middle,length,nstart,nlast,nlow,in);
          if temp3*temp1<0.0,
             last=middle;
             temp2=temp3;
          elseif temp1*temp3>0.0,
             first=middle;
             temp1=temp3;
          end
    end
    root=middle;
else
    flag = 1;
end
```

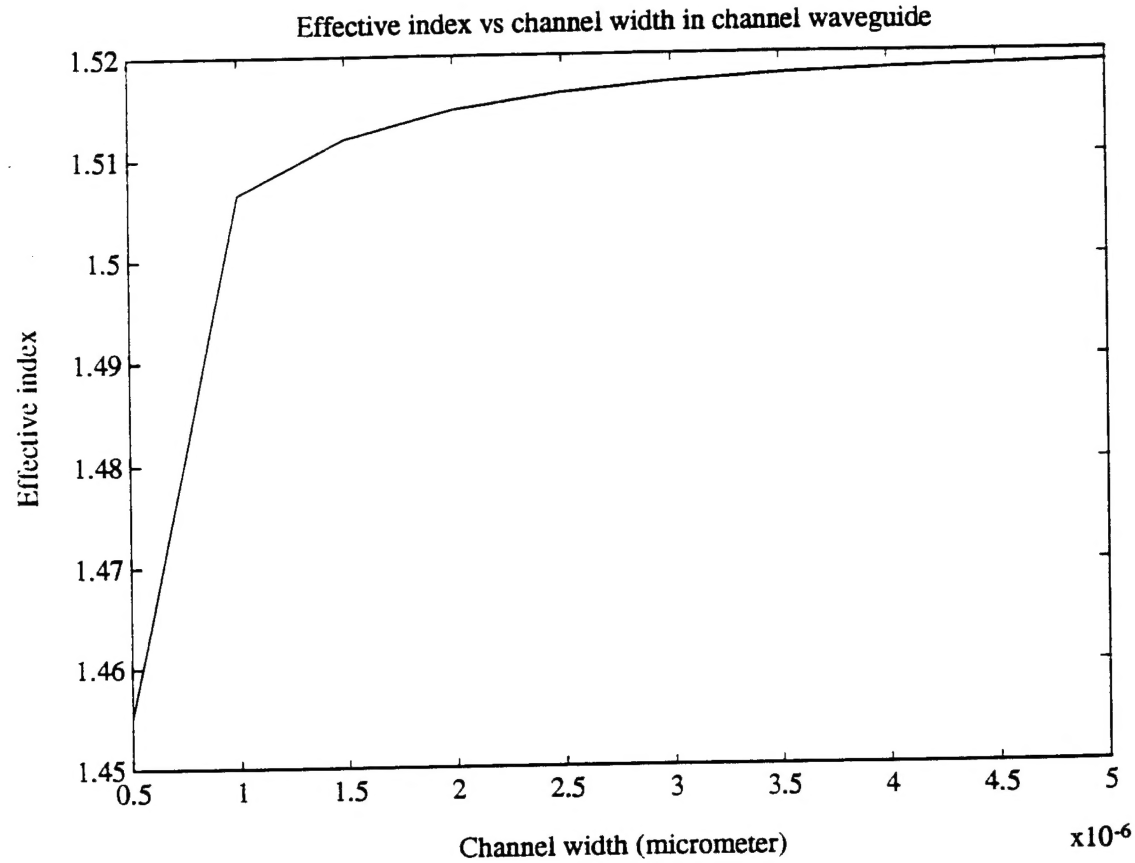
```
function[value] = dismetal(neff,t,n3,n2,n1,m)

% Wavelength of the light source in free space
lambda = 633e-9;
k = 2*pi/lambda;

% permittivities of the meidum
e0 = 8.85e-12;
e1 = (n1)*e0;
e2 = (n2^2)*e0;
e3 = (n3^2)*e0;
eeff = (neff^2)*e0;

% normalized frequency parameter
v = k*t*sqrt((e2-e3)/e0);

% Normalized b parameter
b = (eeff - e3)/(e2-e3);
if b == 1
   b1 = inf;
else
   b1 = 1.0/(1-b);
end

% Asymmetry measure for TE modes
a = (e3-e1)/(e2-e3);

% Eigen equation for TE modes
value = m*pi + atan(sqrt(b*b1)) + atan(sqrt((b+a)*b1)) - v*sqrt(1-b);
```

```
% Initial parameters
im = sqrt(-1);
c = 3.0e+8;
height = 1.0e-6;
width = 1.0e-6;
lambda = 633e-9;
omega = c/lambda;
k = 2*pi/lambda;
mu = 1.2555e-6;

% Region I and Region III refractive inices
n11 = -47.56;
n21 = 1.9;
n31 = 1.484;

% Calulation of effective indices for region I and III (vertical)
l = 0;
[alpha,pointer] = bisectmet(n31,n21,n11,height,l);

while pointer == 0
      solution1(l+1) = alpha;
      l = l + 1;
      [alpha,pointer] = bisectmet(n31,n21,n11,height,l);
end


% Region II refractive indices (vertical)
n12 = 1.0;
n22 = 1.9;
n32 = 1.484;

% Calulation of effective indices for region I and III (vertically)
m = 0;
[alpha,pointer] = bisectmet(n32,n22,n12,height,m);

while pointer == 0
      solution2(m+1) = alpha;
      m = m + 1;
      [alpha,pointer] = bisectmet(n32,n22,n12,height,m);
end


% Calulation of effective indices of the rectangular waveguide
for j = 1:m
    o = 0;
```

```
    n1 = solution1(j);
    n3 = solution1(j);
    n2 = solution2(j);
    [alpha,pointer] = bisectmet(n1,n2,n3,width,o);

    while pointer == 0
          solution(j,o+1) = alpha;
          o = o + 1;
          [alpha,pointer] = bisectmet(n1,n2,n3,width,o);
    end
end
```

```
function [value] = TE(neff)

% Wavelength of the light source
lambda = 633e-9;
k = 2*pi/lambda;


% Thickness of the slab
t = 0.5e-6;
im = sqrt(-1);

% Refractive indices of the supersubstrate, core and the
% substrate respectively.
n1 = 1.2 - 7*im;
n2 = 1.9;
n3 = 1.46;

% Parameters used in the equation
q = k*sqrt(neff^2 - n1^2);
h = k*sqrt(n2^2 - neff^2);
p = k*sqrt(neff^2 - n3^2);

% Eigen equation for the TE mode
value = tan(h*t+2*m*pi) - h*(p+q)/(h^2-p*q);
```

```
global m

% Initial parameters
im = sqrt(-1);
c = 3.0e+8;
n1 = 1.5;
n2 = 1.52;
n3 = 1;
lambda = 633e-9;
omega = c/lambda;
k = 2*pi/lambda;
mu = 1.2555e-6;

ti=0.5e-6;
m = 0;
for i = 1:10
    thick(i) = ti;
    height = ti;
    [alpha,pointer] = bisect(n3,n2,height);
    solution(i) = alpha;
    ti=ti+0.5e-6;
end

plot(thick,solution)
```


Effective index vs channel width in channel waveguide
Effective index
1.52
1.51
1.5
1.49
1.48
1.47
1.46
1.45
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Channel width (micrometer)
x10-6